WHAT IS CLAIMED IS:

1. A storage system comprising:

a plurality of first logical units connected to a host device which form interfaces for the host device;

a storage device for storing therein information received from the host device;

a plurality of second logical units connected to said storage device which form interfaces for said storage device;

a cache memory device for temporarily storing therein data transferred between said plurality of first logical units and said plurality of second logical units; and

a common bus mutually wired between said plurality of first logical units, said plurality of second logical units and said cache memory device.

2. A storage system as set forth in claim 1, wherein said first logical units, second logical units and said cache memory device are made in the form of modules, and each of said modules is detachably mounted to said common bus.

3. A storage system as set forth in claim 1, wherein said common bus is disposed on a back plane, and said first logical units, second logical units and said cache,memory device in the form of modules are detachably mounted to said back plane.

4. A storage system as set forth in claim 1, wherein said host devices having different interfaces are connected to said plurality of first logical units.

5. A storage system as set forth in claim 1, wherein said storage device has a plurality of small-size storage units, said small-size storage units arranged in a horizontal direction form an ECC group, and said ECC group is arranged in a vertical direction.

6. A storage system comprising:

a plurality of duplexed first logical units connected to a host device which form interfaces for the host device;

a storage device for storing therein information received from said host device;

a plurality of duplexed second logical units connected to said

storage device which form interfaces for said storage device;

a duplexed cache memory device for temporarily storing therein data transferred between said plurality of second logical units and said plurality of first logical units; and

a common bus mutually wired between said plurality of first logical units, said plurality of second logical units and said cache memory device.

7. A storage system as set forth in claim 6, wherein said first logical units second logical units and daid cache memory device are made in the form of modules, and each of said modules is detachably mounted to said common bus.

8. A storage system as set forth in claim 6, wherein said common bus is disposed on a back plane, and said first logical units, second logical units and said cache memory device in the form of modules are detachably mounted to said back plane.

9. A storage system as set forth in claim 6, wherein said storage device has a plurality of small-size storage units, said small-size storage units arranged in a horizontal direction form an ECC group, and said ECC

group is arranged in a vertical direction.

10. A storage system as set forth in claim 6, wherein said host device is connected to said common bus through two or more of said plurality of first logical units.

11. A storage system as set forth in claim 1, wherein said storage device is connected to said common bus through two or more of said plurality of second logical units.

12. A storage system as set forth in claim 6, wherein said plurality of first logical units and said plurality of second logical units have each a duplexed microprocessor and a checker for performing comparison in operation between said duplexed microprocessor.

13. A storage system as set forth in claim 6, wherein said common bus has a high-speed I/O bus divided into 2 channels for data transmission and a single-channel multi-processor bus for transmission of control information for said data transmission.

14. A storage system as set forth in claim 13, wherein, when one of the 2 channels in said high-speed I/O bus becomes faulty, the other normal channel is used to continue the operation.

15. A storage system as set forth in claim 13, wherein, when said multi-processor bus becomes faulty, one of said 2 channels in said high-speed I/O bus is used as the multi-processor bus and operation of the high-speed I/O bus is continued by the other channel.

16. A storage system comprising:

a plurality of duplexed first logical units connected to a host device which form interfaces for the host device;

a storage device for storing therein information received from said host device;

a plurality of duplexed second logical units connected to said storage device which form interfaces for said storage device;

a duplexed cache memory device for temporarily storing therein data transferred between said plurality of first logical units and said plurality of second logical units; and

a common bus mutually wired between said plurality of first logical

units, said plurality of second logical units and said cache memory device,

wherein said plurality of first logical units, said plurality of second logical units and said cache memory device allow hot replace with respect to said common bus.

17. A storage system as set forth in claim 16, wherein said first logical units, second logical units and said cache memory device are made in the form of modules, and each of said modules is detachably mounted to said common bus.

18. A storage system as set forth in claim 16, wherein said common bus is disposed on a back plane, and said first logical units, second logical units and said cache memory device in the form of modules are detachably mounted to said back plane.

19. A storage system as set forth in claim 16, wherein said storage device has a plurality of small-size storage units, said small-size storage units arranged in a horizontal direction form an ECC group, and said ECC group is arranged in a vertical direction.

20. A storage system as set forth in claim 16, further comprising a power bus connected with said plurality of first logical units, said plurality of second logical units, said cache memory device, and said storage device and also comprising a multiplexed power source part for supplying power to said power bus and a duplexed power supply part for supplying power to said multiplexed power source part, and wherein the number of power sources in said power source part corresponds to a number necessary for said plurality of first logical units, said plurality of second logical units, said cache memory device, and said storage device plus one.